A miniaturized Ka-band MMIC high-gain medium power amplifier in coplanar line technique by using a conventional 0.5 μm MESFET technology

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Abstract

This paper presents a miniaturized Ka-band MMIC high-gain medium power amplifier in coplanar line technique by using a conventional 0.5 μm GaAs-MESFET technology. To our knowledge a MESFET amplifier with 7 dB gain at Ka-band has never been shown before. In the frequency band 26.3 GHz to 28.3 GHz, the input and output return losses are better than 10 dB. The 1 dB compression point P_{1dB} is higher than 23 dBm at 26.5 GHz. The single ended one-stage amplifier occupies a chip-size of 0.46 x 0.64 mm².

Introduction

The purpose of this work is to investigate a small sized low cost Ka-band MMIC power amplifier in coplanar line technique by using a conventional 0.5 μm MESFET technology. The miniaturized MESFET amplifier is fabricated on a GaAs substrate in CPW-technique. The coplanar technology can be realized without via-hole technique and no backside preparation is required [1]. Using this technology and by miniaturization of the chip size, the low cost and large volume production of MMICs becomes possible [2]. The coplanar elements, like transmission lines, MIM-capacitors, steps, and T-junctions, which are used in the amplifier, are calculated with the quasi-static finite difference method [3, 4]. The amplifier design has been performed with the HP-EEsof Libra software including the coplanar element library and by using the CURTICE cubic model for the MESFET [5, 6, 7]. The MESFET model was extracted by scientists of the IMST [8].

MMIC-Design and Results

Figure 1 shows a simplified circuit diagram of the amplifier and the corresponding photograph is illustrated in Figure 2. The technology of [9] has been used as foundry. The amplifier was designed and optimized for high-gain, good input and output return losses, medium output power, and small chip-size.

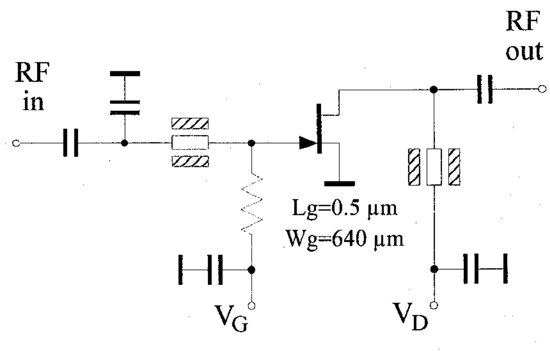

Fig. 1: Simplified circuit diagram of the one-stage 0.5 μm MMIC MESFET amplifier.

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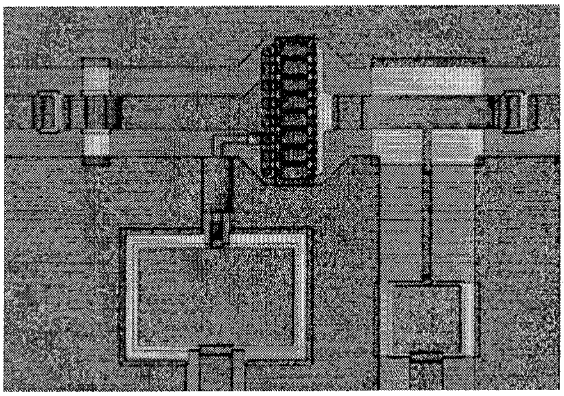

Fig. 2: Photo of the coplanar Ka-band MESFET amplifier (Chip-size: 0.46 x 0.64 mm²).

The amplifier is realized using a 16 gate finger MESFET. Each of the gate fingers has a width of 40 μm. Coplanar transmission lines and MIM-capacitors were utilised for the matching networks. The one-stage amplifier occupies a chip area of 0.295 mm², including bias elements.

The Ka-band amplifier was measured with a combined on-wafer linear and nonlinear measurement system up to 60 GHz [10]. A comparison of the simulated and measured small signal parameters of the Ka-band amplifier is shown in Figure 3 for one bias point.

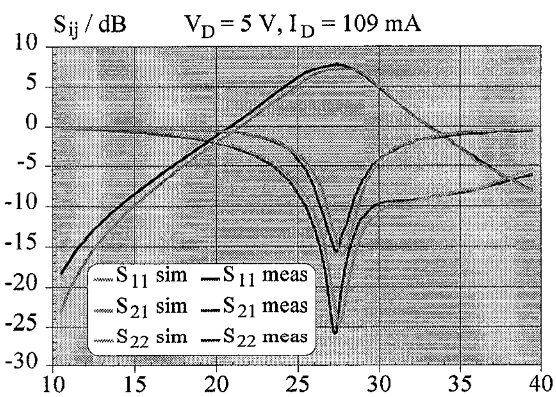

Fig. 3: Comparison of the simulated and measured small signal parameters of the 0.5 μm MESFET Ka-band amplifier.

The amplifier circuit has been biased at a drain voltage of 5 V and a drain current of 109 mA. The agreement between theorical and practical results is excellent. In the frequency band from 26.3 GHz to 28.3 GHz, the input and output reflection coefficients are less than -10 dB and the gain is better than 7 dB with a ripple of 1 dB. The circuit is unconditionally stable (K > 1) over the whole frequency range. Reverse isolation of the amplifier is better than 15 dB in the entire measurement frequency range.

Figure 4 depicts the comparison of the simulated and measured output power and power added efficiency (PAE) versus input power at the frequency 26.5 GHz. The simulated and measured performances agree well. The bias point in this case is V_D = 6 V and V_G = -0.5 V, the measured P_{1dB} is 21.5 dBm with a power added efficiency of 18 %.

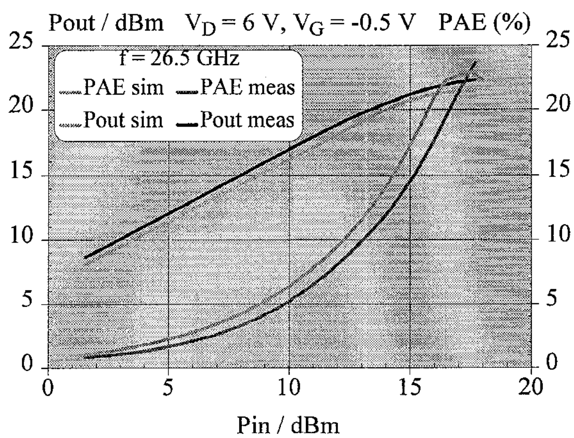

Fig. 4: Comparison of the simulated and measured output power and power added efficiency versus input power at 26.5 GHz.

In Figure 5, the measured 1 dB compression point P_{1dB} versus frequency for different drain voltages and for a fixed gate voltage of V_G = -0.5 V is presented. It can be seen, that the bias point V_D = 6 V and V_G = -0.5 V offers the highest P_{1dB} at 26.5 GHz.

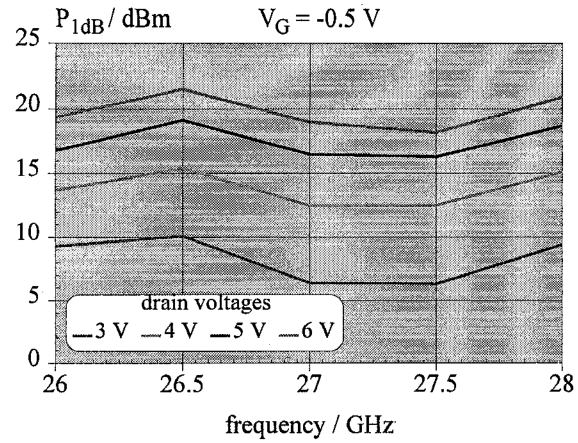

Fig. 5: The 1 dB compression point P_{1dB} versus frequency for different drain voltages and for a fixed gate voltage of V_G = -0.5 V.

Higher drain voltage will increase the output power. Therefore Figure 6 shows the measured output power and power gain versus input power for the drain voltages of V_D = 6 V and V_D = 8 V and for a fixed V_G = -0.5 V. The 1 dB compression point P_{1dB} is increased to 23.5 dBm for the higher drain voltage with a decrease in power gain.

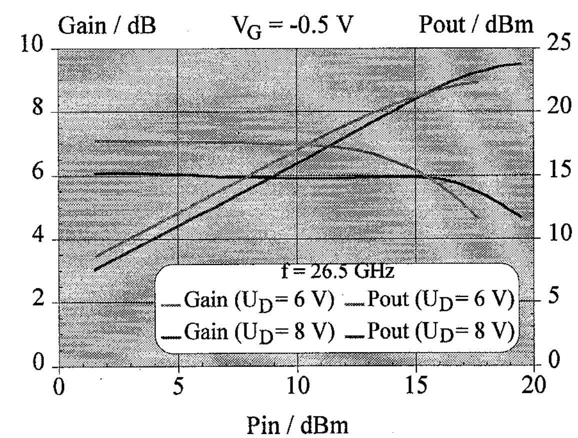

Fig. 6: Power gain and output power versus input power at 26.5 GHz for the drain voltages V_D = 6 V and V_D = 8 V and for a fixed gate voltage of V_G = -0.5 V.

Figure 7 illustrates the P_{1dB} versus the drain voltage at 26.5 GHz for different gate voltages. At this frequency, the variation of the gate voltages has a negligible influence on the power performance. In contrast, the measurements at 28 GHz show a different behavior. At this frequency, the 1 dB compression point P_{1dB} is moderately dependent on the gate voltage, which can be seen from Figure 8.

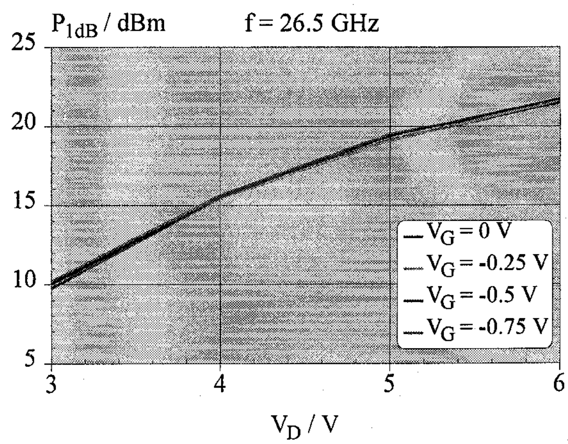

Fig. 7: The 1 dB compression point P_{1dB} versus drain voltage at 26.5 GHz for different gate voltages.

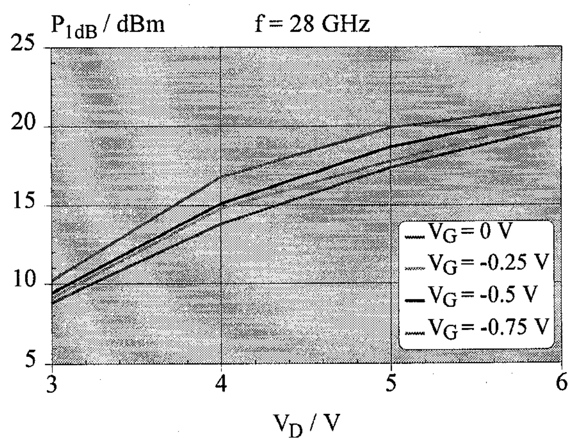

Fig. 8: The 1 dB compression point P_{1dB} versus drain voltage at 28 GHz for different gate voltages.

Conclusion

A miniaturized Ka-band MMIC high-gain medium power amplifier has been realized in coplanar line technique by using a conventional 0.5 μm GaAs-MESFET technology. The single ended one-stage amplifier occupies a chip area of 0.295 mm^2. In the frequency band 26.3 to 28.3 GHz, the gain is betterr than 7 dB and the return losses are better than 10 dB. The 1 dB compression point P_{1dB} is higher than 23 dBm at 26.5 GHz. By means of a coplanar technology combined with the coplanar line techniques and by using a conventional 0.5 μm GaAs-MESFET, medium power amplifier circuits up to Ka-band can be successfully realized. The miniaturization of the chip size yields in a low cost and large volume production.

Acknowledgement

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